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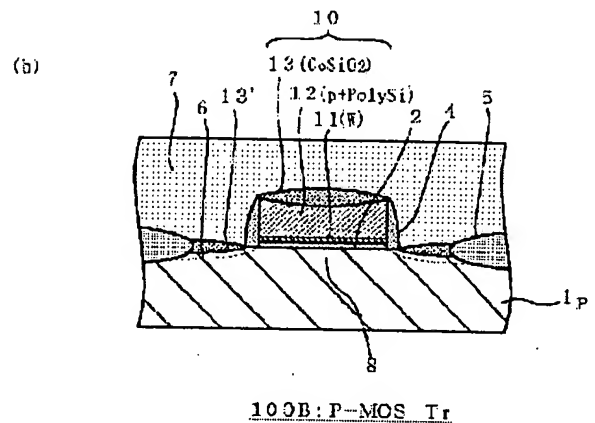
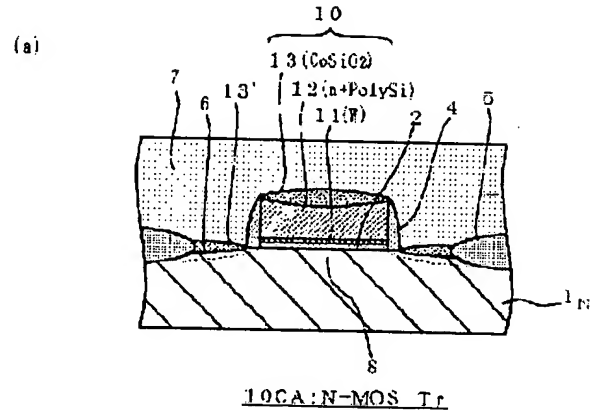
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H01L 29/786 // C23C 16/06

TITLE : MIS TRANSISTOR AND METHOD FOR
MANUFACTURING THE SAME



ABSTRACT : PROBLEM TO BE SOLVED: To freely and continuously control a work function viewed from the gate insulating film side of a gate electrode to a value different from the characteristic value of the materials of the gate electrode, and to continuously control V_{th} in an MIS type transistor.

SOLUTION: In MIS transistors 100A and 100B, a gate electrode 10 is formed like the laminated configuration of a plurality of kinds of metallic layers 11, 12, and 13 whose work functions are different, and the first metallic layer 11 brought into contact with the gate insulating film 2 is formed with not more than film thickness of 5 Debye length by an atomic layer CVD.

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.....型 及 製造方法

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21/285

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617 L

617 J

617 M

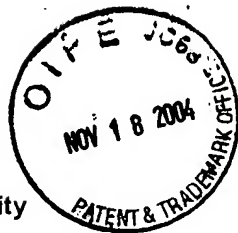
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(54) [Title of Invention]

MIS TYPE TRANSISTOR AND ITS
MANUFACTURING METHOD

(51) [International Patent Classification, 7th Edition]

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21/285

29/43

29/786

// C23C 16/06

[FI]

H01L 21/285 C

C23C 16/06

H01L 29/78 301 G

617 L

617 J

617 M

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 BF07 BF11 BF14 BF15 BF17 BF21 BF28 BG08
 BG28 BG34 BK21 BK34 CB01 CB08 CF04

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 20 BA 22 BA 29 BB11 BB12 LA15 4M104 AA01 AA09
 BB13 BB14 BB16 BB17 BB18 BB40 CC05 DD04 DD43
 DD45 DD72 DD84 DD91 EE03 EE09 EE14 EE16 FF 13 FF
 14 GG09 HH20 5F110 AA08 BB04 CC02 DD05 DD13 EE02
 EE04 EE14 EE15 EE45 FF 01 FF 02 FF 04 GG02 GG12
 NN62 NN66 5F140 AA00 AA06 AB03 AC36 BA 01 BD09
 BD11 BD12 BF07 BF11 BF14 BF15 BF17 BF21 BF28 BG08
 BG28 BG34 BK21 BK34 CB01 CB08 CF04

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氏名又 * 名称 *

田治米 登 * 外 * 名 *

Abstract

(57) 要約 *

課題 *

MIS 型 * * * * * 電極 * * *
 * 絶縁膜側 * * 見 * 仕事関数 * * * * * 電
 極 * 材料 * * * 特性値 * * 異 * * 値 * 自由 *
 連続的 * 制御 * * * * * V_{th} * 連続的 * 制
 御 * * *

解決手段 *

MIS 型 * * * * * 100A * 100B * * * * *
 * 電極 10 * * 仕事関数 * 異 * * 複数種 * 金属
 層 11 * 12 * 13 * 積層構造 * * * * * 絶縁
 膜 2 * 接 * * 第 1 * 金属層 11 * * 原子層 CVD
 * * * * 膜厚 5 * * * 長以下 * 形成 * * *

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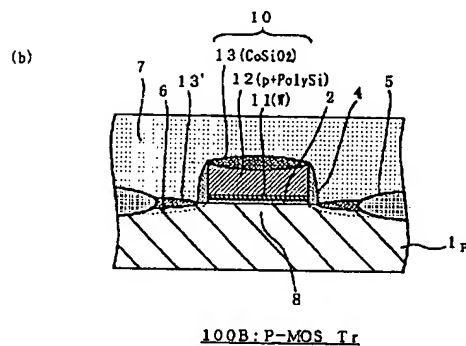
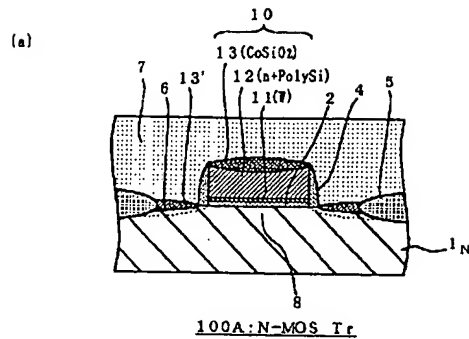
(57) [Abstract]

[Problems to be Solved by the Invention]

In MIS type transistor, characteristic value where material of gate electrode has work function which was seen from gate insulating film side of gate electrode, in value which differs it controls freely in continuous, it controls V_{th} in the continuous with that.

[Means to Solve the Problems]

In MIS type transistor 100A, 100B, it designates gate electrode 10, as laminated structure of metal layer 11, 12, 13 of multiple kinds where work function differs, it forms below film thickness 5debye length the first metal layer 11 which at same time touches to gate insulating film 2, with atomic layer CVD.



Claims

特許請求の範囲

請求項 1

電極、仕事関数、異、複数種、金属層、積層構造、有、絶縁膜、接、第 1 金属層、原子層 CVD (Atomic Layer Chemical Vapour Deposition: ALCVD)、膜厚 5、長以下、形成、特徴、MIS 型

請求項 2

第 1 金属層、膜厚 0.6、長以上、請求項 1 記載、MIS 型

請求項 3

電極材料、積層、電極、形成、MIS 型、製造方法、電極材料、第 1 金属層、絶縁膜上、原子層 CVD、膜厚 5、長以下、形成、上、第 1 金属層、異、金属種、第 2 金属層、積層、特徴、MIS 型、製造方法

請求項 4

第 1 金属層、膜厚 0.6、長以上、形成、請求項 3 記載、製造方法

[Claim(s)]

[Claim 1]

first metal layer where gate electrode, has laminated structure of metal layer of multiple kinds where work function differs, at same time touches to gate insulating film, the MIS type transistor, which designates that it is formed below film thickness 5debye length by the atomic layer CVD (Atomic Layer Chemical Vapour deposition: ALCVD), as feature

[Claim 2]

MIS type transistor, which is stated in Claim 1 where film thickness of first metal layer is 0.6 debye lengths or more

[Claim 3]

manufacturing method, of MIS type transistor which designates that second metal layer of metal type where first on gate insulating film forms first metal layer below film thickness 5debye length with the atomic layer CVD, it laminates gate electrode material, in manufacturing method of MIS type transistor which forms gate electrode, as gate electrode material, differs from first metal layer on that is laminated as feature

[Claim 4]

manufacturing method, of MIS type transistor which is stated

・請求項 3 記載・ MIS 型・ ・ ・ ・ ・ 製造方法・

Specification

・発明・詳細・説明・

0001・

・発明・属・技術分野・

本発明・半導体/絶縁膜/金属・積層構造・有・ MIS 型・ ・ ・ ・ ・ 絶縁膜側・見・ ・ ・ ・ 電極・仕事関数・連続的・制御・ ・ ・ ・ ・ 閾値 V_{th} ・制御・技術・関・

0002・

・従来・技術・

・ ・ ・ Si 基板・形成・ ・ ・ MIS 型・ ・ ・ ・ ・
・ 図 4(a)・(b)・示・ N-MOS ・ ・ ・ ・ ・
P-MOS ・ ・ ・ ・ ・ 一般・ Si 基板・
N ・ ・ ・ I_N 又・ P ・ ・ ・ I_P 上・ ・ ・ 絶縁膜 2
・形成・ ・ ・ 絶縁膜 2 上・ ・ ・ n+PolySi
又・ p+PolySi ・ ・ ・ ・ 電極 3_N ・ 3_P ・積層
・構造・有・ ・ ・ ・

・ ・ 図中・符号 4 ・ ・ ・ 電極・ ・ ・ ・ ・
・ ・ ・ 符号 5 ・ LOCOS ・ ・ ・ 素子分離膜
・ ・ ・ 符号 6 ・ 拡張・ ・ ・ 又・ 拡張・ ・ ・ 領域
・ ・ ・ 符号 7 ・ 層間絶縁膜・ ・ ・ ・

0003・

従来・ ・ ・ ・ ・ 閾値 V_{th} ・ ・ ・ ・ ・
部 8 ・ 不純物濃度・ ・ ・ ・ 制御・ ・ ・ ・ ・

・ ・ ・ 部 8 ・ 不純物濃度制御・ $0.18 \mu m$ 程度・ ・ ・ ・ LSI ・ ・ ・ ・ 注入技術・短時間熱処理技術・ ・ 駆使・ ・ 比較的良好・行・ ・ ・ ・ ・

0004・

・ ・ ・ $0.1 \mu m$ ・ ・ ・ ・ 以降・ ・ ・ ・ ・
・ ・ ・ ・ ・ ・ ・ ・ ・ ・ ・ 不純物量・ ・ ・ V_{th} ・ 制御・ ・ 手法・ ・ ・ ・ ・
長・短・ ・ ・ ・ ・ 1 個当・ ・ ・ ・ ・
・ V_{th} ・ 寄与・ ・ 不純物・絶対数・少・ ・ ・
・統計的・ ・ ・ ・ V_{th} ・ ・ ・ ・ 無視・ ・ ・ ・ ・ (T.Mizuno et al, "Performance Fluctuations of $0.10 \mu m$ MOSFETs - Limitation of $0.1 \mu m$ ULSIs"等, Symp. on VLSI Technology '94) ・

in Claim 3 which forms the first metal layer above film thickness 0.6debye length

[Description of the Invention]

[0001]

[Technological Field of Invention]

It tries this invention, to be able to control work function of gate electrode which was seen from gate insulating film side in MIS type transistor which possesses laminated structure of the semiconductor /insulating film /metal , in continuous , technology which controls threshold value V_{th} of transistor with that it regards.

[0002]

[Prior Art]

MIS type transistor which was formed to bulk Si substrate , Figure 4 (a) , like N- MOS transistor , P-MOS transistor which is shown in (b) , generally, forms gate insulating film 2 in Nwell 1_{N_N} of Si substrate , or on Pwell 1_{P_P} furthermore has possessed structure which laminates gate electrode 3_{N_N} , 3_{P_P} which consists of n+PolySi or p+PolySi on the gate insulating film 2.

Furthermore, as for in the diagram , sign 4 with sidewall of gate electrode , as for the sign 5 with element-isolating film , as for sign 6 with extended source or the extended drain region , as for sign 7 it is a interlayer insulating film with LOCOS .

[0003]

Until recently, threshold value V_{th} of this transistor is controlled with impurity concentration of channel part 8.

impurity density control of channel part 8, freely using ion implantation technology and short time thermal processing technology , is done relatively satisfactorily to LSI of design rule of $0.18 \mu m$ extent .

[0004]

However, regarding $0.1 \mu m$ or design rule transistor of after that, with technique which controls V_{th} with amount of impurity of channel , as channel length becomes short, absolute number of impurity which contributes to V_{th} of transistor of per each decreases, It has become not be able to ignore variation of V_{th} with the statistical fluctuation , (Symp. on VLSI technology '94 such as T.Mizuno et al, "Performance Fluctuations of $0.10 \mu m$ MOSFETs - Limitation of $0.1 \mu m$ ULSIs").

.....部・不純物濃度制御・他・
 ・電極・仕事関数・
 Vth・制御・.....・微細・
 ・対応・.....・切望・

0005・

一方・SOI(Silicon on Insulator)基板・用・
・活性 SOI 層・数十 nm・薄・
 ・・0.25 μm 程度・
 ・不純物濃度制御・.....・Vth・制御・原理
 的・限界・.....

.....部・不純物濃度・例・ $1 \times 10^{18} \text{cm}^{-3}$ 以上・高濃度・.....・不純物散乱・
 増大・伴・.....・移動度・低下・
 電流駆動能力・低下・.....・Vth・SOI・
 膜厚依存性・増大・無視・.....・好・

.....SOI 基板・用・
・電極・仕事関数・
 ・Vth・制御・.....・切望・

0006・

.....他.....・電極・低抵抗化.....・電極・
 空乏化防止等.....・電極・金属・形成
必要・
Vth.....・電極・仕事関数・制御・
制御.....望・

0007・

・発明・解決.....・課題・

.....・電極・材料・決・
閾値 Vth.....
 構造(.....不純物濃度.....絶縁膜・膜
 厚等).....必然的・決.....・電極
 ・単・金属・形成・場合.....一種類・Vth
 ・有.....作製・
問題・

0008・

.....対.....・電極・材料.....多結晶
 TiN・配向性・変化.....同・材料・用・
仕事関数・種.....値・制御・試・行
(K.Nakajima et al, 1999 Symposium
 on VLSI Technology Digest of Technical Papers,
 p95(1999))・

.....手法.....制御.....仕事関
 数・範囲・基本的・結晶方位.....仕事関
 数・差・範囲内(通常・0.1V 程度.....)・制限・

Then, other than impurity density control of channel part, to try to be able to control Vth of transistor even with work function of gate electrode, as process of fine device correspondence it is designed in such a way that it is desired.

[0005]

On one hand, because with transistor which uses SOI (silicon-on-insulator) substrate, the activity SOI layer several tens of nm is thin, regarding design rule of 0.25 μm extent, with impurity density control in control of Vth there is a limit in principle.

In addition, when impurity concentration of channel part, is designated as high concentration above for example $1 \times 10^{18} \text{cm}^{-3}$, because mobility of carrier decreases attendant upon increase of impurity scattering, because current drive capacity can decrease, furthermore, cannot ignore increase of film thickness dependency of SOI of Vth and becomes it is not desirable.

Then, regarding transistor which uses SOI substrate, it is desired that the Vth of transistor is controlled with work function of gate electrode.

[0006]

Because of depletion prevention or other of resistance-lowering, gate electrode of this other things and gate electrode, it is designed in such a way that is needed that gate electrode is formed with metal, it is desired Vth even because of that that it controls with control of work function of the gate electrode.

[0007]

[Problems to be Solved by the Invention]

But, when material of gate electrode is decided, because threshold value Vth of the transistor is decided inevitably with device structure (film thickness etc of channel impurity concentration, gate insulating film) of transistor, when the gate electrode is formed simply with metal, there is a problem that only the transistor which possesses Vth of one kind it is possible to produce.

[0008]

K.Nakajima et al, 1999 symposium on VLSI technology Digest of Technical Papers, p95 (1999). orientation of polycrystalline TiN changing vis-a-vis this, as material of the gate electrode, making use of same material although, attempt which controls work function in various value being done, it is

But, because with this technique, range of work function which can be controlled, in basic to (Usually, to 0.1 V extent) inside range of difference of the work function is restricted

.....仕事関数・連続的・制御.....
原理的・課題.....多結
 晶・配向・100%制御.....不可能・近・
微細.....応用・考.....場
 合.....再現性・歩留.....点.....課題・多

0009・

.....本発明者.....酸化膜上.....電
 極.....CVD法.....等.....島
 状領域・形成・次・島状領域上.....島状
 領域・構成材料.....異.....材料・薄膜・積層
場合・島状領域・薄膜.....酸化膜
 ・対.....被覆率等・変化.....
 ・電極・仕事関数・変化.....手法・提案.....
 ・(特開平 7-211896 号公報).....

.....手法.....微細化
 ・伴・島状領域・被覆率.....1.....
 内・平均化.....特性.....増大.....
問題.....

0010・

以上.....従来技術・対.....本発明・MIS
 型.....電極.....絶
 縁膜側.....見・仕事関数.....電極・
 材料.....特性値.....異.....値・自由・連続
 的・制御..... V_{th} ・連続的・制御・
目的.....

0011・

課題・解決.....手段・

本発明者.....仕事関数・異.....複数種・金
 属・積層膜・用.....MIS型.....
 ・電極・形成.....場合.....絶縁膜・接・
 ・第1・金属層・膜厚・5.....長(即・数原
 子層)以下・薄・形成.....上・第2・金属層
 ・積層.....絶縁膜側.....見・実効的
 ・仕事関数・第1・金属層・固有・仕事関
 数・第2・金属層・固有・仕事関数.....間・
 連続的・制御.....場合・第1・金属
 層・原子層 CVD(Atomic Layer Chemical
 Vapour Deposition: ALCVD).....形成.....
 5.....長以下.....薄膜.....所定・膜
 厚・再現性・安定的・形成.....見出

0012・

即.....本発明.....電極・仕事関数・異
 ・複数種・金属層・積層構造・有.....
 ・絶縁膜・接・第1・金属層・原子層
 CVD.....膜厚・5.....長以下・形成.....
特徴.....MIS型.....提供

with crystal orientation, there to be a principle problem that, it is not possible to control work function in continuous, in addition, because which orientation of polycrystalline 100% is controlled is close to impossible, when of application to microscopic transistor was thought, problem is many even from point of reproducibility and yield.

[0009]

In addition, in this inventor on gate oxide film, first forming island region which consists of silicon etc with CVD method as gate electrode, next, laminating thin film with material which constituent material of island region differs on island region, island region in this case and coating ratio etc for gate oxide film of thin film changing depending, work function of gate electrode technique which changes is proposed, (Japan Unexamined Patent Publication Hei 7-211896 disclosure).

But, in this technique, coating ratio of island region, averaging is not done inside device of one attendant upon narrowing of device, there is a problem that variation of characteristic increases.

[0010]

Like above vis-a-vis Prior Art, characteristic value where material of gate electrode has work function which was seen from gate insulating film side of gate electrode in the MIS type transistor, in value which differs it controls this invention, freely in the continuous, it designates that it tries to be able to control V_{th} in continuous with that as objective.

[0011]

[Means to Solve the Problems]

When when gate electrode of MIS type transistor is formed making use of laminated film of metal of multiple kinds where work function differs, film thickness of first metal layer which touches with gate insulating film it forms these inventors, thin 5 debye long (Namely, several atomic layers), or less laminates second metal layer on that, effective work function which was seen from gate insulating film side, In first metal layer in work function and second metal layer of peculiar between work function of peculiar it can control in continuous, in case of this, when first metal layer is formed with atomic layer CVD (Atomic Layer Chemical Vapour deposition: ALCVD), even with thin film, 5 debye lengths or less fact that reproducibility well it can form in stable was discovered in predetermined film thickness.

[0012]

Namely, as for this invention, gate electrode, has laminated structure of metal layer of the multiple kinds where work function differs, first metal layer which at same time touches to gate insulating film, offers MIS type transistor which designates that it is formed below film thickness 5 debye length

...

0013

本發明...絕緣膜上...電極材料...積層...電極形成...MIS型...製造方法...電極材料...第1金屬層...絕緣膜上...原子層CVD...膜厚5...長以下...形成...上...第1金屬層...異...金屬種...第2金屬層...積層...特徵...MIS型...製造方法...提供...

0014

發明・實施・形態

以下圖面参照...本發明詳細說明...

各圖中同一符號同一又同等構成要素表...

0015

圖1(a)(b)...本發明MIS型...一實施形態示N-MOS又P-MOS...100A 100B模式的斷面圖...

100A 100B...Si基板...N... 1_N 又P... 1_P 上... SiO_2 ...絕緣膜2上形成...電極10...絕緣膜2側... (W) ...第1金屬層11...n+PolySi又p+PolySi...第2金屬層12... $CoSi_2$...第3金屬層13...積層構造有...

圖中符號13'...第3金屬層13...同種金屬擴張...又擴張...領域6上形成...金屬層...

0016

第1金屬層11...膜厚0.6...長~5...長(即...0.1原子層~數原子層)形成...

第2金屬層12...PolySi...濃度 $\sim 5 \times 10^{20} \text{ cm}^{-3}$... $(P)(N-MOS \text{ Tr} : 100A)$ 又...素 $(B)(P-MOS \text{ Tr} : 100B)$...完全導電體(n+PolySi又p+PolySi)...膜厚50~300nm形成...

第3金屬層13...10~100nm形成...

0017

by atomic layer CVD, as feature.

[0013]

In addition, first on gate insulating film forms first metal layer below film thickness 5debye lengthwith atomic layer CVD, this invention laminates gate electrode material on gate insulating film, in the manufacturing method of MIS type transistor which forms gate electrode, as gate electrode material, offers the manufacturing method of MIS type transistor which designates that second metal layer of metal type whichdiffers from first metal layer on that is laminated as feature.

[0014]

[Embodiment of the Invention]

While below, referring to drawing, you explain this invention in detail.

Furthermore, each in the diagram, same sign has displayed same or equal component.

[0015]

Figure 1 (a), (b) is schematic sectional view of N- MOS or P-MOS transistor 100A, 100B whichshows one embodiment of MIS type transistor of respective this invention.

As for this transistor 100A, 100B, gate electrode 10 which was formed on gate insulating film 2 whichconsists of Nwell 1_N of bulk Sisubstrate or SiO_2 ₂ on Pwell 1_P, from gate insulating film 2 side, has had laminated structure of metal layer 13 of 3 rd which consist of second metal layer 12 and $CoSi_2$ ₂ which consist of first metal layer 11 and n+PolySi or p+PolySi which consist of [tansuguten] (W).

Furthermore, in the diagram, sign 13' is extended source or metal layer which wasformed on extended drain region 6 with metal layer 13 of 3 rd and metal of same kind.

[0016]

Here, first metal layer 11 is formed to film thickness 0.6debye long - 5 debye long (Namely, 0.1 atomic layer ~several atomic layers).

second metal layer 12 completely conductor (n+PolySi or p+PolySi) with being something which is done phosphorus of concentration $\sim 5 \times 10^{20} \text{ cm}^{-3}$ (P) (N- MOS Tr :100A) or by doped doing boron (B) (P-MOS Tr :100B) in PolySi, is formed to film thickness 50~300nm.

In addition, metal layer 13 of 3 rd is formed to 10 - 100 nm.

[0017]

..... 100A・100B 本發明
 ・ ・ ・ 第 1 ・ 金屬層 11 ・ 膜厚 ・ 5 長以
 下 ・ 薄 ・ 形成 電極 10
 ・ ・ ・ 絕緣膜 2 側 ・ 見 ・ 実効的 ・ 仕事関数 ・ ・
 第 1 ・ 金屬層 11 ・ 金屬種 ・ ・ ・ 定 ・ 仕事関
 数 ・ 第 2 ・ 金屬層 12 ・ 金屬種 ・ ・ ・ 定 ・ 仕事
 関数 ・ 中間 ・ 仕事関数 値
 ・ 第 1 ・ 金屬層 11 ・ 膜厚 連續的 ・ 変
 化 所期 ・ 値

・ ・ ・ ・ ・ 第 1 ・ 金屬層 11 ・ 膜厚 ・ 制御 ・ ・ ・ ・ ・
 ・ 仕事関数 ・ 制御 ・ ・ ・ ・ ・ 第 ・ 金屬層 11
 ・ ・ ・ ・ ・ 第 2 ・ 金屬層 12 ・ 影響 ・ ・ ・ ・ ・
 ・ ・ ・ ・ ・ 第 1 ・ 金屬層 11 ・ 膜厚 ・ 1 ・ ・ ・ ・ ・
 長増 ・ ・ ・ ・ ・ 絶縁膜 2 側 ・ 見 ・ 第 2
 ・ 金屬層 12 ・ 影響 ・ $1/e$ 急激 減少 ・ 第 1
 ・ 金屬層 11 ・ 膜厚 ・ 5 ・ ・ ・ ・ 長 超 ・ ・ ・ ・ ・
 ・ 絶縁膜 2 側 ・ 見 ・ 仕事関数 ・ ・ 第 2 ・
 金屬層 12 ・ 影響 ・ 實質的 ・ 現 ・ ・ ・ ・ ・
 ・ ・ ・ (Appl.Phys.Lett.,54(3),p268(1989)参照)

0018 ▪

第 1 金屬層 11 薄形成場合
第 1 金屬層 11 1 原子層未滿即金屬
原子連續層離散的互重
合絕緣膜上形成

0019 •

本發明・第1・金屬層11・絶縁膜2
上・膜厚・原子層・制御・形成・
・原子層CVD・第1・金屬層11・構成
原子・1層・以下・膜厚・堆積

原子層 CVD ・ ・ 従来 ・ MBE(Molecular Beam
Epitaxy) ・ ・ 異 ・ ・ ・ 必 ・ ・ ・ 下地 ・ 結晶基板
・ 必要 ・ ・ ・ ・ ・ ・ 超高真空 ・ 必要 ・ ・
・ ・ ・ ・ ・ SiO₂ 等 ・ 非晶質 ・ ・ ・ 絶縁膜上
・ 制御性 ・ ・ 原子層 ・ ・ ・ 薄膜 ・ 成長 ・ ・
・ ・ ・ ・ ・ ・ ・ ・ ・ ・ ・ ・

0020 -

・原子層 CVD ・分子(Precursor) ・
吸着 ・対 ・大 ・場合 ・分子 ・吸
着時 ・未吸着 ・
分子 ・吸着 ・1 ・操作 ・1 原子層
・堆積 ・通常 0.1 原子層(0.6
・長)程度 ・堆積 ・数 ・重 ・
・1 原子層 ・堆積 ・

Like this transistor 100A, 100B, with this invention, to make work function of intermediate of the work function which becomes settled due to metal type of work function and the second metal layer 12 which become settled effective work function which was seen from gate insulating film 2 side of gate electrode 10 film thickness of first metal layer 11 by forming thin 5 debye lengths or less, due to metal type of first metal layer 11, furthermore, value with film thickness of first metal layer 11 changing in continuous, It makes anticipated value.

this way whenever as for being able to control work function with control of film thickness of first metal layer 11, influence of second metal layer 12 because the shield it is done, film thickness of first metal layer 11 1 debye length increases with first metal layer 11 when, influence of second metal layer 12 which was seen from gate insulating film 2 side decreases to $1/e$ suddenly, film thickness of first metal layer 11 exceeds 5 debye length, in work function which was seen from gate insulating film 2 side, Because influence of second metal layer 12 stops appearing substantially, (Applied Physics Letters, 54 (3), p268 (1989) reference).

[0018]

Furthermore, when first metal layer 11 is formed thin, first metal layer 11 under 1 atomic layer, namely, metal atom not to be a continuous layer, to discrete, may be formed on gate insulating film mutually stacking without being agreeable.

[0019]

With this invention, in order on gate insulating film 2 controlling film thickness with the atomic layer level, to form first metal layer 11, with atomic layer CVD, it accumulates 1 layer or film thickness of less than that at a time constituent atom of first metal layer 11.

As for atomic layer CVD, crystal substrate not to be always done necessity in the substrate conventional MBE (Molecular Beam Epitaxy) unlike, in addition, because either ultrahigh vacuum isn't needed, on gate insulating film of SiO_2 or other amorphous controllability thin film it can grow well with atomic layer level.

[0020]

In addition, with atomic layer CVD, when gas molecule (Precursor) it is large vis-a-vis adsorption site, because unadsorbed site mask it is done when adsorbing of gas molecule, gas molecule it is not case that 1 atomic layer accumulates with operation of 1 cycle which adsorbs, usually, 0.1 atomic layer (0.6 debye length) extent accumulate, means with that 1 atomic layer accumulates by repeating the number of cycles.

..... 数・制御
 的・金属層・膜厚・制御
 ・可能 (Surface chemistry of materials
 deposition at atomic layer level, Tuomo Suntola,
 Applied Surface Science 100:101, 391-398(1996)
 参照)・

0021・

本発明 第1・金属層11・膜厚・下
 限 絶縁膜2側 見・仕事
 関数・制御 点 格別制限

..... 原子層 CVD ・被吸着体 分子
 ・吸着 1 被吸着体・堆
 積 原子層・膜厚・下限値(通常・0.1 原子
 層) 第1・金属層11・膜厚・實際上・下限
 値

0022・

第1・金属層11・膜厚・制御
 絶縁膜2側 見 電極10・仕事関数
 ・制御・具体例 例 第1・金属
 層11・3原子層程度 絶縁膜2
 ・ 見・仕事関数・N-MOS
 100A・P-MOS 100B 共
 W膜・有 仕事関数 ϕ_M ・4.55eV 程度
 ・第1・金属層11・1原子層程度 場合
 絶縁膜2 見・仕事関数 ϕ_M ・
 4.55eV・近・値 第1・金属層11・
 膜厚・0.1原子層程度 W原子
 ・絶縁膜2・表面・被覆・被覆率 比
 例 絶縁膜2側 見・仕事関数 ϕ_M
 ・線形的・変化 N-MOS
 100A W膜・仕事関数 ϕ_M ・
 4.1~4.55eV・制御 P-MOS
 100B 4.55~5.2eV・制御

..... 第1・金属層11・膜厚・0.5原子
 層程度 N-MOS
 100A 仕事関数 ϕ_M ・4.3eV 程度
 P-MOS 100B 仕事関数 ϕ_M ・
 4.9eV 程度

0023・

本発明 第2・金属層12 上述
 100A・100B 絶縁膜2
 側 見・仕事関数 第3・金属層13・影
 響・現 厚・形成 必要
 ・応 絶縁膜2側 見・仕事関数
 ・第1・金属層11・第2・金属層12
 第3・金属層13・影響・現

Therefore, by fact that number of cycles is controlled, it
 becomes possible to control film thickness of metal layer in
 digital, (Surface chemistry of materials deposition at atomic
 layer level, Tuomo Suntola, Applied Surface Science
 100/101, 391-398 (1996) reference).

[0021]

Regarding to this invention, there is not exception restriction
 from the point which controls work function which you saw
 from gate insulating film 2 side concerning lower limit of film
 thickness of first metal layer 11.

Because of this, with 1 cycle which gas molecule adsorbs
 into the suffering adsorbant with atomic layer CVD, lower
 limit (Usually, 0.1 atomic layer) of film thickness of atomic
 layer which is accumulated in suffering adsorbant, becomes
 really lower limit on film thickness of first metal layer 11.

[0022]

When with control of film thickness of first metal layer 11,
 for example first metal layer 11 is designated as 3 atomic layer
 extent as embodiment of control of work function of gate
 electrode 10 which was seen from gate insulating film 2 side,
 even with when work function which was seen from the gate
 insulating film 2 both N-MOS transistor 100A, P-MOS
 transistor 100B, becomes 4.55 eV extent of work function : ϕ_{M_M}
 which W film of bulk has, designates first
 metal layer 11 as 1 atomic layer extent, work function : ϕ_{M_M}
 which was seen from gate insulating film 2
 reaches value which is close to 4.55 eV, but when film
 thickness of first metal layer 11 is designated as 0.1 atomic
 layer extent, W atom almost being proportionate to the
 coating ratio which surface of gate insulating film 2 sheath is
 done, work function : ϕ_{M_M} which was seen from
 gate insulating film 2 side it to be possible to change in
 linear, with N-MOS transistor 100A, Be able to control work
 function : ϕ_{M_M} of W film in 4.1 - 4.55 eV, it can
 control with P-MOS transistor 100B in 4.55 - 5.2 eV.

Therefore, it depends on designating film thickness of first
 metal layer 11 as 0.5 atomic layer extent, work function : ϕ_{M_M}
 can designate with N-MOS transistor 100A
 as 4.3 eV extent, with P-MOS transistor 100B can designate
 work function : ϕ_{M_M} as 4.9 eV extent.

[0023]

Regarding to this invention, like above-mentioned transistor
 100A, 100B, in order in work function which was seen from
 gate insulating film 2 side, for influence of metal layer 13 of 3
 rd not to appear, it is possible to form second metal layer 12,
 thickly, but in work function which was seen from according
 to need, gate insulating film 2 side, it is possible not only a
 first metal layer 11 and a second metal layer 12, that influence

.....

.....場合.....第2金属層12.....原子層CVD.....数原子層以下.....形成.....

0024

第3金属層13.....電極10.....低抵抗化.....注入時.....注入.....不純物.....下.....注入.....形成時.....等.....必要.....応.....設.....

0025

本發明.....MIS型.....製造方法.....上述.....第1金属層11.....原子層CVD.....形成.....公知.....方法.....例.....図1(a).....N-MOS.....100A.....図2.....示.....製造.....

0026

(1).....Si基板14.....公知.....手法.....LOCOS法.....素子分離膜5.....N..... I_N形成.....(図2(a)).....

0027

(2)次.....絶縁膜2..... SiO_2例.....1.5~4.0nm程度成長.....(図2(b)).....

0028

(3).....絶縁膜2上.....原子層CVD.....第1金属層11.....W膜.....膜厚0.6.....長~5.....長(即.....0.1原子層~数原子層)堆積.....(図2(c)).....

.....場合.....原子層CVD条件.....例.....基板温度.....300 deg C.....分子(Precursor)..... $WOCl_4$使用..... $WOCl_4$ 流入..... N_2 排気..... H_2 流入..... N_2 排気.....工程.....繰返.....

0029

(4)第1金属層11(W膜)上.....PolySi.....通常.....CVD.....膜厚50~300nm堆積.....N-MOS.....形成領域.....P.....例.....20keV.....濃度 $5 \times 10^{15} cm^{-2}$打込.....n+PolySi.....形成.....第2金属層12.....(図2(d)).....

.....P-MOS.....形成.....場合.....形成領域.....B.....例.....加速電圧.....

of metal layer 13 of 3 rd appears.

In that case, with atomic layer CVD it forms also second metal layer 12, below several atomic layers.

[0024]

metal layer 13 of 3 rd, as for sake of of resistance-lowering of gate electrode 10 or according to need is provided etching stopper etc at time of mask, contact formation which impurity which is filled at time of ion implantation tries is not filled that under gate.

[0025]

As manufacturing method of MIS type transistor of this invention, above-mentioned way other than forming first metal layer 11 with atomic layer CVD, it can do thing with known method as shown in Figure 2, it can produce N-MOS transistor 100A of for example Figure 1 (a).

[0026]

(1) First, in bulk Si substrate 14, with technique of public knowledge element-isolating film 5 and the Nwell I_{N_N} are formed with LOCOS method (Figure 2 (a)).

[0027]

(2) Next, $SiO_{₂}$, for example 1.5~4.0nm extent it grows as gate insulating film 2 (Figure 2 (b)).

[0028]

Figure 2 (c). On (3) gate insulating film 2, W film film thickness 0.6 debye long - 5 debye long (Namely, 0.1 atomic layer ~ several atomic layers) is accumulated with atomic layer CVD, as first metal layer 11

In case of this, atomic layer CVD condition designates for example substrate temperature as 300 deg C, uses $WOCl_{₄}$ gas molecule (Precursor) as, $WOCl_{₄}$ influx, $N_{₂}$ exhaust, $H_{₂}$ influx and the $N_{₂}$ exhaust repeats step gas [furooshiikuensu] as.

[0029]

Figure 2 (d). On (4) first metal layer 11 (W film), film thickness 50~300nm it accumulates PolySi with conventional CVD, in order furthermore, in forming region of N-MOS transistor Pion, to become concentration $5 \times 10^{15} cm^{-2}$ with for example 20keV, ramming down, it forms n+PolySi, this the second metal layer 12 does

Furthermore, when P-MOS transistor is formed, in order Bion, with the for example acceleration voltage 10keV, to

10keV ・ 濃度 $5 \times 10^{15} \text{cm}^{-2}$ ・ ・ ・ ・ ・ 打 ・ 込
 ・ ・ p+PolySi ・ 形成 ・ ・ ・

N-MOS ・ ・ ・ ・ ・ 形成領域 ・ P-MOS ・ ・ ・
 ・ ・ ・ ・ 形成領域 ・ ・ ・ ・ 打 ・ 分 ・ ・ ・ ・
 ・ ・ ・ ・ ・ 15 ・ 用 ・ ・ ・

0030 ・

(5) ・ ・ 後 ・ 公知 ・ 手法 ・ ・ ・ ・ ・ 電極 10 ・
 ・ ・ ・ ・ 形成 ・ 拡張 ・ ・ ・ ・ 又 ・ 拡張 ・ ・ ・ ・
 領域 6 ・ 不純物 ・ 注入 ・ ・ ・ ・ 電極 10 ・ ・ ・
 ・ ・ ・ ・ 4 ・ 形成 ・ ・ ・ ・ S 及 ・ ・ ・ ・ D
 ・ ・ 不純物 ・ 注入 ・ 活性化 ・ 行 ・ ・ CoSi_2 ・ ・
 ・ ・ 金屬層 13 ・ 13' ・ 第 2 ・ 金屬層 12 上及 ・
 拡張 ・ ・ ・ ・ 又 ・ ・ ・ ・ 領域 6 上 ・ 自己整合の
 ・ 形成 ・ 層間絶縁膜 7 ・ 堆積 (図 2(e)) ・ ・ ・
 ・ ・ ・ ・ ・ 形成 ・ ・ ・ ・ 充填 ・ 配線 ・ 形成
 ・ 順次行 ・ 半導体装置 ・ 完成 ・ ・ ・ ・

0031 ・

図 3 ・ ・ 本発明 ・ 異 ・ 態様 ・ MIS 型 ・ ・ ・ ・
 ・ ・ 100C ・ 模式的断面図 ・ ・ ・ ・

・ ・ ・ ・ ・ 100C ・ ・ 第 1 ・ 金屬層 11 ・
 Ti ・ 形成 ・ 第 2 ・ 金屬層 12 ・ Pt ・ 形成
 ・ 第 3 ・ 金屬層 ・ 省略 ・ ・ ・ ・

0032 ・

・ ・ ・ ・ ・ 100C ・ ・ ・ ・ ・ 形成
 成 ・ 基板 ・ ・ SOI 基板 9 (図中 ・ 符号 16 ・
 埋 ・ 込 ・ 酸化膜 ・ 表 ・) ・ 使用 ・ 完全空乏型
 ・ ・ ・ ・ ・ ・ ・ ・ ・ ・ 部 8 ・ 不純物 ・ ・
 ・ ・ ・ ・ ・ ・ ・ ・ ・ ・ 電極 10 ・ 仕事関数 ・
 ・ ・ V_{th} ・ 制御 ・ ・ ・ ・ ・

・ ・ ・ ・ V_{th} ・ 制御 ・ ・ ・ ・ N-MOS ・ ・ ・ ・
 ・ ・ P-MOS ・ ・ ・ ・ ・ 形成 ・ 場合 ・ ・ ・
 ・ ・ ・ ・ 電極 ・ 仕事関数 ・ 不純物濃度 ・
 調整 ・ ・ ・ ・ 別 ・ ・ 設定 ・ ・ ・ ・ ・
 第 1 ・ 金屬層 11 ・ 膜厚 ・ N-MOS ・ ・ ・ ・
 ・ P-MOS ・ ・ ・ ・ ・ 制御 ・ ・ ・
 ・ ・ ・ ・ ・ N-MOS ・ ・ ・ ・ ・ P-MOS ・
 ・ ・ ・ ・ 双方 ・ ・ ・ ・ 所期 ・ V_{th} ・ 実現 ・
 ・ ・ ・ ・ ・

0033 ・

本発明 ・ MIS 型 ・ ・ ・ ・ ・ 種 ・ ・
 態様 ・ ・ ・ ・ ・

第 1 ・ 金屬層 11 ・ 第 2 ・ 金屬層 12 ・ 第 3 ・ 金
 屬層 13 ・ 構成 ・ 金屬 ・ 種類 ・ 適宜変更 ・ ・
 ・ ・ ・ ・ ・ 例 ・ ・ 第 1 ・ 金屬層 11 ・ 上述 ・
 W 又 ・ Ti ・ 代 ・ ・ Mo ・ Ta ・ Zr 等 ・ 高融点金

become concentration $5 \times 10^{15} \text{cm}^{-2}$ in forming region, ramming down, it forms the p+PolySi.

resist mask 15 is used to forming region of N-MOS transistor and inside dividing of ion of forming region of P-MOS transistor.

[0030]

Figure 2 (e), formation of contact hole, fullness of metal and formation of wiring sequential doing semiconductor device is completed. It forms pattern of gate electrode 10 (5) after that, with technique of the public knowledge, fills impurity to extended source or extended drain region 6, forms sidewall 4 of gate electrode 10, fills impurity to source S and the drain D, and it activates, on second metal layer 12 and in extended source or on drain region 6 it forms metal layer 13, 13'; which consists of CoSi_2 in self-aligning, interlayer insulating film 7 is accumulated

[0031]

Figure 3 is schematic sectional view of MIS type transistor 100C of embodiment where this invention differs.

With this transistor 100C, first metal layer 11 is formed from Ti, second metal layer 12 is formed from Pt, metal layer of 3rd is abbreviated.

[0032]

In addition, this transistor 100C uses SOI substrate 9 (in the diagram, sign 16 displays buried oxide film.) as substrate which forms the transistor, like complete empty type transistor it is something where controls V_{th} with only work function of gate electrode 10 without doped doing impurity in channel part 8.

this way when V_{th} is controlled, when N-MOS transistor and the P-MOS transistor are formed, it is not possible to set work function of those gate electrode separately with adjustment of impurity concentration. Because film thickness of first metal layer 11 can be controlled with each one of the N-MOS transistor and P-MOS transistor, anticipated V_{th} can be actualized in both parties of N-MOS transistor and P-MOS transistor.

[0033]

Furthermore can MIS type transistor of this invention, take various embodiment.

As for types of metal which metal layer 13 of first metal layer 11, second metal layer 12, 3rd configuration is done it is possible, replaces for example first metal layer 11 to above-mentioned W or Ti, is possible to form from Mo, Ta,

属・形成・

・場合・第1・金属層11・形成・
原子層CVD・使用・分子(Precursor)・
・対応・金属・化物・
・化物・有機金属化合物・使用・

・分子・大・応・原子層CVD・1・
・堆積・金属層・膜厚・
・変・数・変化・
・第1・金属層11・所望・膜厚・制御・

0034・

第2・金属層12・第1・金属層11・構成
金属・種類・応・定・例
・Pt・Pd・Co・Ir等・形成・

0035・

・本発明・MIS型・
上述・電極10・積層構造・形成・
・以外・電極・他・構造・
・等・構造・特・制限・
・公知・種・MIS型・広・適用・

・絶縁膜2・種類・Si酸化膜・限・Si
窒化酸化膜・Ta₂O₅・Al₂O₃等・高誘電体膜・
使用・膜厚・適宜変更・

0036・

・発明・効果・

本発明・MIS型・電
極・仕事関数・異・複数種・金属層・積層
構造・金属層・絶縁膜・接
・層・原子層CVD・膜厚5・長
以下・薄膜・形成・絶縁膜側・
・見・電極・仕事関数・電極・
材料・固有・値・別個・連続的・自由・制
御・

・閾値V_{th}・
・不純物・制御・場合・比・1・
・対・不純物・個数・統計的・
揺・V_{th}・低減・
・V_{th}・電源電圧共・低・設定・可
能・

・半導体装置・低電力化・高速化・図・

Zr or other high melting point metal to modify appropriately.

In case of this, in order to form first metal layer 11, oxyhalide, halide, organometallic compound of the metal which corresponds gas molecule which is used with atomic layer CVD (Precursor) as, can be used.

According to size of gas molecule, film thickness of metal layer which can accumulate with 1 cycle of atomic layer CVD it changes first metal layer 11 can be controlled in desired film thickness, but number of cycles by changing.

[0034]

It is possible to decide according to types of constituent metal of the first metal layer 11 but, it can form second metal layer 12, from for example Pt, Pd, Co, Ir etc.

[0035]

In addition, regarding MIS type transistor of this invention, above-mentioned way other than forming gate electrode 10 in laminated structure, concerning other structure and source, drain or other structure of gate electrode there is not especially restriction, can apply to various MIS type transistor of public knowledge widely.

types of gate insulating film 2 or not just Sio₂ film, be able to use the Sinitriding oxide film, Ta₂O₅, Al₂O₃ or other ferroelectric membrane, film thickness it can modify appropriately.

[0036]

[Effects of the Invention]

According to MIS type transistor of this invention, to designate gate electrode as the laminated structure of metal layer of multiple kinds where work function differs, because the layer which touches to inside gate insulating film of metal layer with atomic layer CVD is formed in thin film below film thickness 5debye length, work function of gate electrode which was seen from gate insulating film side, in material of gate electrode can be controlled separately with value of peculiar freely in continuous.

Therefore, when controls threshold value V_{th} of transistor with only impurity of channel, comparing, it is possible to decrease variation of the V_{th} with statistical fluctuation of number of impurity for the transistor of one both V_{th}, power supply voltage it becomes possible to set low.

Depending, it is possible to assure low electric power

.....	conversion and acceleration of semiconductor device .
図面・簡単・説明・	[Brief Explanation of the Drawing(s)]
図・・	[Figure 1]
本発明・MIS型・・・・・・モードの断面図・	It is a schematic sectional view of MIS type transistor of this invention .
図・・	[Figure 2]
本発明・MIS型・・・・・・製造方法・工程 説明図・・・・・・	It is a step explanatory diagram of manufacturing method of MIS type transistor of this invention .
図・・	[Figure 3]
本発明・他・態様・MIS型・・・・・・モード の断面図・・・・・・	It is a schematic sectional view of MIS type transistor of other embodiment of this invention .
図・・	[Figure 4]
従来・MOS型・・・・・・モードの断面図	It is a schematic sectional view figure of conventional MOS type transistor .
符号・説明・	[Explanation of Symbols in Drawings]
10	10
・・電極	gate electrode
100A	100A
実施例・・・・・・	transistor of Working Example
100B	100B
実施例・・・・・・	transistor of Working Example
100C	100C
実施例・・・・・・	transistor of Working Example
11	11
第1・金属層	first metal layer
12	12
第2・金属層	second metal layer
1N	1<SB>N</SB>
N・・・・	Nwell
1P	1<SB>P</SB>
P・・・・	Pwell
2	2
・・絶縁膜	gate insulating film
4	4
・・・・・・	sidewall
5	5

素子分離膜

element-isolating film

6

6

拡張・・・又・拡張・・・領域

Extended source or extended drain region

7

7

層間絶縁膜

interlayer insulating film

9

9

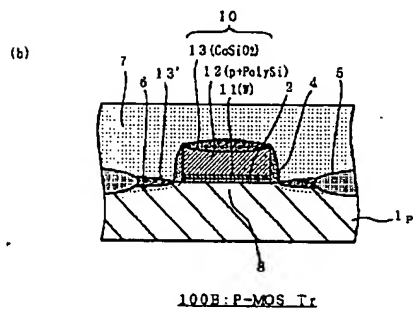
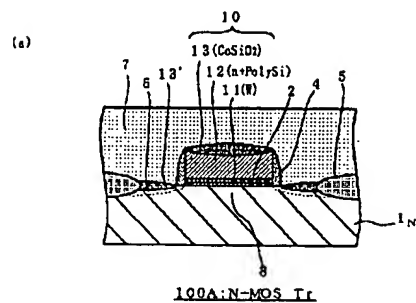
SOI 基板

SOI substrate

Drawings

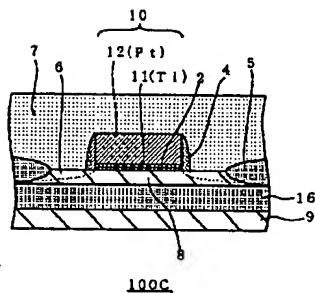
図・・・

[Figure 1]



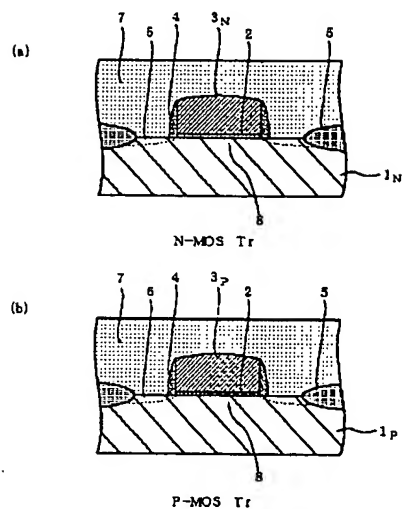
図・・・

[Figure 3]



図・・・

[Figure 4]



[Figure 2]

